Amendment to the Claims:

This listing of claims will replace all prior versions, and listing, of claims in the application.

Listing of Claims:

1. (canccled)

2. (canceled)

3. (currently amended): A circuit, comprising:

a delay locked loop having a delay line with a plurality of tap outputs;

a first tap selection circuit that produces a first set of tap addresses to select a first set of the plurality of tap outputs from the delay line according to a first timing to produce a first output signal;

a second tap selection circuit that produces a second set of tap addresses to select a second set of the plurality of tap outputs from the delay line according to a second timing to produce a second output signal;

a modulator combining the first and second output signals to produce a modulated output signal; and

~~The apparatus according to claim 2,~~

wherein the modulator frequency- modulates the first output signal with the second output signal.

4. (currently amended): A circuit, comprising:

a delay locked loop having a delay line with a plurality of tap outputs;

a first tap selection circuit that produces a first set of tap addresses to select a first set of the plurality of tap outputs from the delay line according to a first timing to produce a first output signal;

a second tap selection circuit that produces a second set of tap addresses to select a second set of the plurality of tap outputs from the delay line according to a second timing to produce a second output signal;

a modulator combining the first and second output signals to produce a modulated output signal; and

~~The apparatus according to claim 2,~~

wherein the modulator phase- modulates the first output signal with the second output signal.

5. (currently amended): A circuit, comprising:

a delay locked loop having a delay line with a plurality of tap outputs;

a first tap selection circuit that produces a first set of tap addresses to select a first set of the plurality of tap outputs from the delay line according to a first timing to produce a first output signal;

a second tap selection circuit that produces a second set of tap addresses to select a second set of the plurality of tap outputs from the delay line according to a second timing to produce a second output signal;

a modulator combining the first and second output signals to produce a modulated output signal; and

~~The apparatus according to claim 2,~~

wherein the modulator amplitude- modulates the first output signal with the second output signal.

6. (canceled)

7. (canceled)

8. (currently amended): ~~The apparatus of claim 1, further comprising:~~ A circuit, comprising:

a delay locked loop having a delay line with a plurality of tap outputs;

a first tap selection circuit that produces a first set of tap addresses to select a first set of the plurality of tap outputs from the delay line according to a first timing to produce a first output signal;

a second tap selection circuit that produces a second set of tap addresses to select a second set of the plurality of tap outputs from the delay line according to a second timing to produce a second output signal;

a tap selection processor that selects the first set of the plurality of tap outputs from the delay line according to the first timing, and selects the second set of the plurality of tap outputs from the delay line according to the second timing, the tap selection processor comprising:

a frequency accumulator receiving an integer part K of K.C where $K.C = F_{out} / F_{ref}$, where F_{out} is a desired output frequency and F_{ref} is a reference clock frequency, and wherein the frequency accumulator is clocked by F_{ref}; and

a phase accumulator that receives the fractional part C of K.C, wherein the phase accumulator is clocked by an overflow of the frequency accumulator, and wherein the frequency accumulator produces the first set of the plurality of tap output addresses as an output thereof;

a first demultiplexer responsive to the tap selection processor to selectively route the selected first set of the plurality of tap outputs to a common node to produce the first output signal; and

a second demultiplexer responsive to the tap selection processor to selectively route the selected second set of the plurality of selected tap outputs to the common node to produce the second output signal.

9. (currently amended): ~~The apparatus according to claim 8,~~ A circuit, comprising:

a delay locked loop having a delay line with a plurality of tap outputs;

a first tap selection circuit that produces a first set of tap addresses to select a first set of the plurality of tap outputs from the delay line according to a first timing to produce a first output signal, the first tap selection circuit further comprising:

a first tap selection processor that selects the first set of the plurality of tap outputs from the delay line according to the first timing; and

a first demultiplexer responsive to the first tap selection processor to selectively route the selected first set of tap outputs to a common node to produce the first output signal;

a second tap selection circuit that produces a second set of tap addresses to select a second set of the plurality of tap outputs from the delay line according to a second timing to produce a second output signal, the second tap selection circuit further comprising:

a second tap selection processor that selects the second set of the plurality of tap outputs from the delay line according to the second timing; and

a second demultiplexer responsive to the second tap selection processor to selectively route the selected second set of tap outputs to the common node to produce the second output signal;

and wherein the first tap selection processor comprises:

a frequency accumulator receiving an integer part K of K.C where $K.C = F_{out} / F_{ref}$, where F_{out} is a desired output frequency and F_{ref} is a reference clock frequency, and wherein the frequency accumulator is clocked by F_{ref}; and

a phase accumulator that receives the fractional part C of K.C, wherein the phase accumulator is clocked by an overflow of the frequency accumulator, and wherein the frequency accumulator produces the first set of the plurality of tap output addresses as an output thereof.

10.(original): The apparatus according to claim 9, wherein the second tap selection processor comprises a phase offset adder receiving the first set of the plurality of tap outputs as a first input and a normalized phase shift as a second input thereto and producing the second set of the plurality of tap output addresses as an output thereof, and wherein the phase offset adder is clocked by the overflow of the frequency accumulator.

11. (currently amended): A circuit for producing two output signals having frequency F_{out} and differing by a phase shift, comprising:

a delay locked loop having a plurality of addressable tap outputs;

a tap selection circuit that selects a first sequence of tap addresses C_{ja}; ~~and~~

an adder that adds a normalized phase shift component $\Phi = \underline{K.C}$ ~~K.C~~ $\alpha / (2\pi)$ (α = a desired phase shift in radians) to the first sequence of tap addresses C_{ja} to produce a second sequence of tap addresses C_{jb}, where C is the fractional part of K.C in K.C = F_{out} / F_{ref}, and F_{ref} being a reference clock frequency; and

a first multiplexer and a second multiplexer, wherein the first sequence of tap addresses C_{ja} are applied to the first multiplexer to produce a first output signal F_{outa}, and wherein the second sequence of tap addresses C_{jb} are applied to the second multiplexer to produce a second output signal F_{outb}, and wherein F_{outa} differs from F_{outb} by the desired phase shift.

12. (canceled)

13. (original): The apparatus according to claim 11, wherein the desired phase shift comprises ±90 degrees.

14. (original): The apparatus according to claim 11, wherein the desired phase shift component Φ comprises a time varying phase shift component.

15. (currently amended): A circuit for producing two output signals differing by a phase shift, comprising:

a delay locked loop having a plurality of addressable delay line tap outputs, the delay locked loop synthesizing the output signals at a frequency F_{out}, with K.C= F_{out} / F_{ref}, and F_{ref} being a reference clock frequency;

a tap selection circuit that selects a sequence of tap addresses C_{ja};

a first multiplexer, wherein the sequence of tap addresses C_{ja} are applied to a plurality of inputs of the first multiplexer to produce a first output signal F_{outa}; ~~and~~

a second multiplexer, wherein the sequence of tap addresses C_{ja} are added to a delay factor ~~αK.C~~ $\alpha/(2\pi)$ where α is a desired phase shift in radians and applied to a plurality of inputs of the second multiplexer to produce a second output signal F_{outb}; and

wherein the first and second multiplexers each comprise N:1 multiplexers having N inputs.

16. (canceled)

17. (original): The apparatus according to claim 15, wherein α corresponds to a fixed phase shift.

18. (original): The apparatus according to claim 15, wherein the α corresponds to ±90 degrees.

19. (original): The apparatus according to claim 15, wherein the α comprises a time varying phase shift.

Claims 20-33 (canceled)

34. (currently amended): A digital frequency modulator, comprising:

a delay locked loop having a delay line with a plurality of tap outputs;

a tap selection processor that selects a sequence of time varying tap addresses $C_j(t)$ that vary in time in accordance with a modulating signal m(t); and

a multiplexer circuit, and wherein the time varying tap addresses $C_j(t)$ are applied to the multiplexer circuit to select a time varying sequence of tap outputs as a frequency modulated output signal $F_{out}(t)$ wherein the tap selection processor comprises an integrator that integrates the modulating signal m(t) and an adder that adds the integrated modulating signal m(t) to a selected sequence of tap addresses C_j to produce $C_j(t)$.

35. (canceled)

36. (original): The apparatus according to claim 34, wherein the time varying tap addresses $C_j(t)$ are further selected to amplitude modulate the output signal $F_{out}(t)$ in accordance with the modulating signal m(t).

37. (original): The apparatus according to claim 34, wherein the time varying tap addresses C(t) are further selected to phase modulate the output signal $F_{out}(t)$ in accordance with the modulating signal m(t).

38. (original): The apparatus according to claim 35, wherein the modulating signal m(t) comprises an analog signal.

39.(original): The apparatus according to claim 34, wherein the modulating signal m(t) comprises a data signal.

40. (currently amended): A digital amplitude modulator, comprising:

a delay locked loop having a delay line with a plurality of tap outputs;

a tap selection processor that selects a sequence of time varying tap addresses $C_j(t)$ that vary in time in accordance with a modulating signal m(t); ~~and~~

a multiplexer circuit, and wherein the time varying tap addresses $C_j(t)$ are applied to the multiplexer circuit to select a time varying sequence of tap outputs as an amplitude modulated output signal $F_{out}(t)$; and

wherein the tap selection processor comprises:

a first adder that adds the modulating signal m(t) to a selected sequence of tap addresses C_{ja} to produce a first sequence of time varying tap addresses $C_{jb}(t)$;

a second adder that subtracts the modulating signal m(t) from the selected sequence of tap addresses C_{ja} to produce a second sequence of time varying tap addresses $C_{jc}(t)$; and

wherein $C_j(t)$ comprises $C_{ja}(t)$ and $C_{jb}(t)$;

and wherein the multiplexer circuit comprises:

a first multiplexer receiving the first sequence of time varying tap addresses $C_{jb}(t)$ to produce a first output signal $V_1(t)$; and

a second multiplexer receiving the second sequence of time varying tap addresses $C_{jc}(t)$ to produce a second output signal $V_2(t)$;

and further comprising:

a summation circuit that adds $V_1(t)$ to $V_2(t)$ to obtain an amplitude modulated output signal V(t);.

41. (canceled)

42. (currently amended): The apparatus according to claim ~~41~~ 40, wherein the adding circuit comprises an analog summation circuit.

43. (original): The apparatus according to claim 42, wherein the summation circuit comprises a three state analog summation circuit.

44. (original): The apparatus according to claim 43, wherein the three state analog summation circuit comprises a NAND gate and a NOR gate, each receiving V1(t) and V2(t) and producing first and second outputs therefrom; and a first and a second transistor connected in series and driven by the first and second outputs respectively to produce a three state output at a node coupling the first transistor with the second transistor.

45. (original): The apparatus according to claim 40, wherein the time varying tap addresses $C_j(t)$ are further selected to frequency modulate the output signal $F_{out}(t)$ in accordance with the modulating signal m(t).

46. (original): The apparatus according to claim 40, wherein the time varying tap addresses C(t) are further selected to phase modulate the output signal $F_{out}(t)$ in accordance with the modulating signal m(t).

47. (original): The apparatus according to claim 40, wherein the modulating signal m(t) comprises an analog signal.

48. (original): The apparatus according to claim 40, wherein the modulating signal m(t) comprises a data signal.

49. (currently amended): A method of producing multiple output frequencies using a delay locked loop having a delay line with a plurality of tap outputs, comprising:

selecting a first sequence of the tap outputs according to a first timing to produce a first output signal F_{out1}; ~~and~~

selecting a second sequence of the tap outputs according to a second timing to produce a second output signal F_{out2}.; and

applying addresses of the first sequence of tap outputs to a first multiplexer to select the first sequence of tap outputs; and

applying addresses of the second sequence of tap outputs to a second multiplexer to select the second sequence of tap outputs; and

modulating the first sequence of tap outputs with the second sequence of tap outputs.

50. (canceled)

51. (canceled)

52. (original): A method of producing two output signals differing by a phase shift in a delay locked loop circuit having a delay line with a plurality of addressable tap outputs, comprising:

selecting a first sequence of tap addresses C_{ja}; and

adding a phase shift component Φ to the first sequence of tap addresses C_{ja} to produce a second sequence of tap addresses C_{jb}.

53. (original): The method according to claim 52, further comprising:

applying the first sequence of tap addresses C_{ja} to a first multiplexer to produce a first output signal F_{outa}; and

applying the second sequence of tap addresses C_{jb} to a second multiplexer to produce a second output signal F_{outb}, and wherein F_{outa} differs from F_{outb} by a phase shift related to Φ.

54. (original): The method according to claim 52, wherein the phase shift comprises ±90 degrees.

55. (original): The method according to claim 52, wherein the phase shift component Φ comprises a time varying phase shift component.

56. (original): A method of producing two output signals differing by a phase shift using a delay locked loop having a plurality of addressable delay line tap outputs, comprising:

selecting a sequence of tap addresses C_{ja};

applying the sequence of tap addresses C_{ja} to a plurality of inputs of a first multiplexer to produce a first output signal F_{outa}; and

applying the sequence of tap addresses C_{ja} to a plurality of inputs of a second multiplexer to produce a second output signal F_{outb};

wherein F_{out1} differs from F_{out2} by the phase shift, and wherein the phase shift is determined by a constant difference in address location selected by the sequence of tap addresses C_{ja} between the first and second multiplexers.

57. (original): The method according to claim 56, wherein the first and second multiplexers are connected to the tap outputs in a manner such that a tap address C_{La} selects an input corresponding to tap number L of the first multiplexer and corresponding to tap number $L+\Phi$ in the second multiplexer, where Φ is a phase shift normalized to a length of the delay line.

58. (original): The method according to claim 57, wherein the sequence of tap addresses C_{ja} is applied to the second multiplexer through a delay element.

589. (currently amended): The apparatus according to claim 56, wherein the phase shift corresponds to ±90 degrees.

60. (original): The apparatus according to claim 56, wherein the phase shift comprises a time varying phase shift.

Claims 61–70 (canceled)

71. (currently amended): A method of providing digital frequency modulation in a delay locked loop circuit having a delay line with a plurality of tap outputs, comprising:

selecting a sequence of time varying tap addresses $C_j(t)$ that vary in time in accordance with a modulating signal m(t), wherein the selecting comprises:

integrating the modulating signal m(t); and

adding the integrated modulating signal m(t) to a selected sequence of tap addresses C_j to produce $C_j(t)$; and

applying the time varying tap addresses $C_j(t)$ to a multiplexer circuit to select a time varying sequence of tap outputs as a frequency modulated output signal $F_{out}(t)$.

72. (canceled)

73. (currently amended): A method of providing digital amplitude modulation in a delay locked loop circuit having a delay line with a plurality of tap outputs, comprising:

selecting a sequence of time varying tap addresses $C_j(t)$ that vary in time in accordance with a modulating signal m(t), wherein the selecting comprises:

adding the modulating signal m(t) to a selected sequence of tap addresses C_{ja} to produce a first sequence of time varying tap addresses $C_{jb}(t)$; and

subtracting the modulating signal m(t) from the selected sequence of tap addresses C_{ja} to produce a second sequence of time varying tap addresses $C_{jc}(t)$, wherein $C_j(t)$ comprises $C_{ja}(t)$ and $C_{jb}(t)$; and

applying the time varying tap addresses $C_j(t)$ to a multiplexer circuit to select a time varying sequence of tap outputs as an amplitude modulated output signal $\Gamma_{out}(t)$.

74. (canceled)

75. (currently amended): The method according to claim ~~74~~ 73, and wherein the applying comprises:

applying the first sequence of time varying tap addresses $C_{jb}(t)$ to a first multiplexer to produce a first output signal $V_1(t)$; and

applying the second sequence of time varying tap addresses $C_{jc}(t)$ to a second multiplexer produce a second output signal $V_2(t)$.

76. (original): The method according to claim 75, further comprising adding $V_1(t)$ to $V_2(t)$ to obtain an amplitude modulated output signal V(t).

77. (original): The method according to claim 76, wherein the adding is carried out in an analog summation circuit.

78. (original): The method according to claim 77, wherein the analog summation circuit comprises a three state analog summation circuit.

79. (original): A method of selecting delay line taps to produce an output signal from a delay locked loop, comprising:

computing an tap address P.Q where P is an integer part and Q is a fractional part; and

selecting a delay line tap address of P during a portion of an operational cycle and of P+1 during a remainder of the operational cycle, with the regularity of selection of P and P+1 determined by an algorithm that establishes an average value of the tap address as approximately P.Q.

80. (original): The method according to claim 79, wherein the algorithm selects the value of P for 0.Q operational cycles and P+1 for 1 - 0.Q operational cycles.